VHDL for Sequential Circuits: Implementing a customized State Machine

Andy Zou

501026732

TA: Jasminder Singh

COE328 Section 12

November 16, 2021

**Introduction**

The purpose of this lab is to learn about the Moore finite state machine and how it functions. This specific finite state machine is programmed to cycle through 9 states which result in set values.

**Results**

Diagram

Description automatically generated with low confidence

**Figure 1:** Block schematic diagram of Moore state machine

Graphical user interface

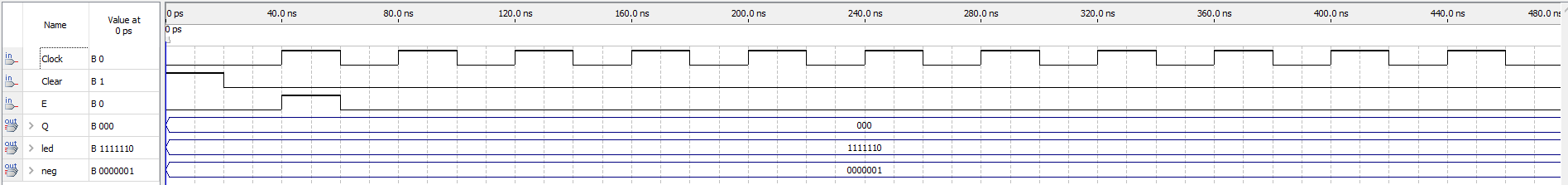
Description automatically generated with low confidence

**Figure 2:** Waveform results of block schematic diagram in Figure 1

Calendar

Description automatically generated

**Figure 3:** Johnson Counter block schematic diagram



**Figure 4:** Waveform for Figure 3

Table

Description automatically generated

**Figure 5:** VHDL code of Moore State machine

Diagram, engineering drawing

Description automatically generated

**Figure 6:** Finite state diagram

**Analysis**

Figure 1 shows the Moore state machine in a block schematic diagram hooked up to a seven seg output. Figure 5 shows the VHDL code of the Moore state machine. Combined, they produced an output seen in Figure 2. It shows the clock being cycled on and off which results in the output displaying numbers corresponding to my student number. Figure 6 shows the logic diagram of the Moore state machine. It produced an output that is correct as the expectations is that it outputs the student number one digit at a time when it cycles through.

Figure 3 shows the Johnson Counter block schematic diagram with the output for the waveform in Figure 4. This part could not get working and the output could not be achieved. Checking over the seven segment, there was nothing wrong with it. Checking through the Johnson code, I could not identify what is going wrong. This is at far as I could get the Johnson’s part to work.